Abstract of the Disclosure:

An integrated dynamic memory includes a memory cell array having memory cells for storing a charge corresponding to an information bit. The memory cell array has a regular cell area with regular memory cells, a first test cell area with first test cells and a second test cell area with second test cells. A control unit is provided for refreshing the charge contents of the regular memory cells with a first refresh time, a control unit is provided for refreshing the charge contents of the first test cells with a second refresh time, and the charge contents of the second test cells with a third refresh time. The first refresh time is shorter than the second refresh time and the latter is shorter than the third refresh time. An evaluation unit is provided for detecting memory cell defects in the first and second test cell areas.

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